MOTOROLA

MBM2011A

1M X 1 BIT MAGNETIC BUBBLE MEMORY DEVICE

Advance Information

GENERAL DESCRIPTION

The MBM2011A is a 1,048,576 (2^{20}) bit magnetic bubble memory device. All required magnetic components, including permanent magnets, the drive field coils and protective magnetic shield are integral parts of the device. The package is a 1.15 x 1.10 x 0.36 inch 16-pin DIP.

The architecture of the MBM2011A features a double-period block-replicate organization with swap gates on the input track. Data storage is organized as 512 storage loops of 2,048 bits each. Additional loops are provided to store the error correction code and as redundant loops. In one of two dedicated map loops on-chip the redundant map loop data is stored.

The MBM2011A magnetic bubble memory can be operated synchronously or asynchronously. Average access time to a page of data is less than 11.5 ms at 100 kHz. Data transfer rate is 100 kilobits per second at 100 kHz. Average power dissipation at 100 kHz is 1.0 W. The device will operate over a case temperature range of 0°C to 70°C, and data is retained without power from −40°C to 100°C.

The device is fabricated using a pseudo-planar process to improve operating margins as well as to enhance reliability. The use of CrCuCr in the conductor elements insures excellent conductivity while greatly increasing resistance to problems associated with electromigration.
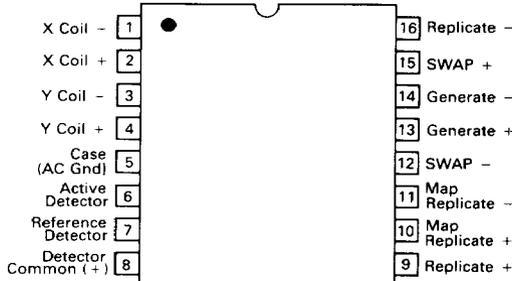
FEATURES

- Non-volatile
- High Density
- Solid State
- Low Power
- Start/Stop Capability
- Page-Oriented Access

- On-Chip Redundant Loop Map
- Swap Gates
- Block Replicate
- Error Correction Code Storage
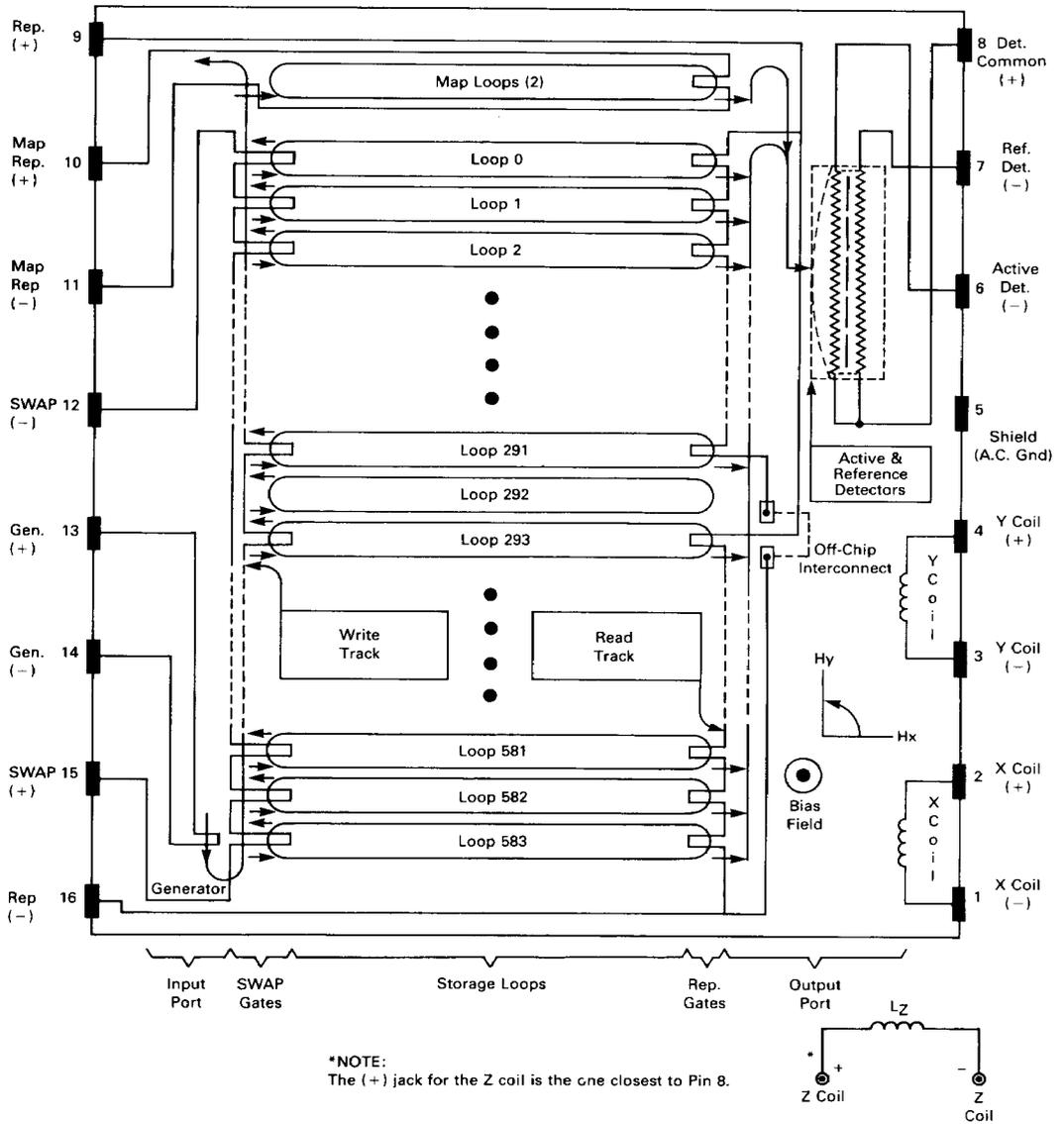- 16-pin Dual-in-Line Package

Bubble

PIN ASSIGNMENTS

X Coil −	1	16	Replicate −
X Coil +	2	15	SWAP +
Y Coil −	3	14	Generate −
Y Coil +	4	13	Generate +
Case (AC Gnd)	5	12	SWAP −
Active Detector	6	11	Map Replicate −
Reference Detector	7	10	Map Replicate +
Detector Common (+)	8	9	Replicate +

FIGURE 1 — BLOCK DIAGRAM

*NOTE:
The (+) jack for the Z coil is the one closest to Pin 8.

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ABSOLUTE MAXIMUM RATINGS

Characteristics	Min	Max	Units
Operating Temperature (Case) (T_C)	0	70	°C
Non-Volatile Storage Temperature	−40	100	°C
Storage Temperature	−40	120	°C
External Magnetic Field	—	20	Oe
Peak Current in X Coil*	—	900	mA
Peak Current in Y Coil*	—	1,100	mA
Peak Current in Z Coil*	—	3,000	mAdc
Peak Replicate Current	—	25	mAdc
Peak Generate Current	—	35	mAdc
Peak Swap Current	—	15	mAdc
Peak Detector Current	—	5.0	mAdc
Coil Disturb Current with Data Retention	—	10	mAdc
Interelement Voltage	—	55	V

*These peak currents are allowed subject to the device temperature not exceeding the temperature limits.

ELECTRICAL CHARACTERISTICS (T_C = 0°C, rotating field frequency (f_o) = 100 kHz)

FUNCTION CURRENTS

Characteristics	Symbol	Min	Typ	Max	Units
Generate Current	I_G	190	—	230	mA
Swap Current	I_S	16	—	20	mA
Data Replicate Cut Current at T_C = 25°C (Note 1)	$I_{RC(25)}$	134	144	154	mA
Data Replicate Transfer Current	I_{RT}	30	—	40	mA
Map Replicate Cut Current at T_C = 25°C (Note 1)	$I_{RCM(25)}$	67	72	77	mA
Map Replicate Transfer Current	I_{RTM}	16	—	20	mA
Map Transfer In Current	I_{TM}	−16	—	−20	mA
Detector Current	I_{DA}, I_{DR}	3.8	4.0	4.2	mA
Temperature Coefficient of Cut Current (Map and Data) Referenced to Value at T_C = 25°C (Note 1)	αRC	−0.32	−0.34	−0.36	%/°C

Note 1: Map and Data replicate cut currents require temperature compensation. The current at any case temperature, T_C, is given by:

$$I_{RC(T)} = I_{RC(25)} [1 + \frac{\alpha RC}{100} (T\text{-}25)] \quad 0 \leq T \leq 70°C \qquad I_{RCM(T)} = I_{RCM(25)} [1 + \frac{\alpha RC}{100} (T\text{-}25)] \quad 0 \leq T \leq 70°C$$

COIL DRIVES (See Figure 2)

| Characteristics	Symbol	Min	Typ	Max	Units
Coil Driver Supply Voltage	V_X, V_Y	11.4	12	12.6	V
Coil Driver Switch on Resistance (2 switches in series)	R_{on}	0.7	—	1.8	Ω
Coil Driver Clamp Diode Drop (2 diodes in series)	V_{clamp}	—	—	1.6	V
X Coil Peak Current (L_x = nom, V_x = nom) (R_{on}, V_{clamp} = nom)	I_{XP}	—	650	—	mA
Y Coil Peak Current (L_y = nom, V_y = nom) (R_{on}, V_{clamp} = nom)	I_{YP}	—	740		mA
Coil Current Offset	I_{xo}, I_{yo}	−10	—	10	mA
Stop Current Overshoot	I_{so}	—	—	+10 −0	mA
Total Coil Power	P_c	—	—	1.4	W
Z-Coil Sensitivity		—	26.5	—	Oe/A
Z-Coil Current to Simultaneously Erase All Data Stored Rotating Field On Rotating Field Off	I_{zap}	2.0 3.0	— —	— —	A
Duration of Erase Current	t_{ZAP}	0.5	—	10	ms

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SCOPE

This specification describes the magnetic, electrical, mechanical and environmental parameters of the 1Mbit magnetic bubble device, MBM2011A as manufactured by Motorola Inc.

DEVICE ORGANIZATION

The 1Mbit bubble memory chip uses a block-replicate organization with swap gates on the input track. The storage area is arranged as 512 storage loops each, with 2,048 bit locations. Additional loops are provided for error correction (12), and defect tolerance (60), giving a total of 584 loops. Data is written and read at the clock frequency which is the rotating field frequency. Figure 1 is a schematic diagram of the 1Mbit chip.

FIGURE 2 — X, Y COIL DRIVE

(a.) TYPICAL DRIVE CIRCUIT
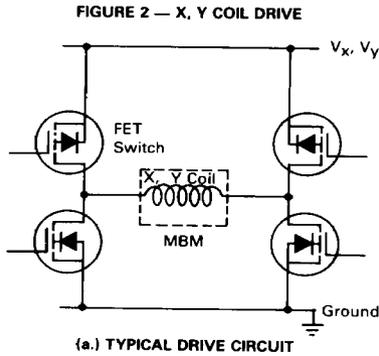
Data Input

To write into the device, the single generator is pulsed and the data pattern is propagated along the double period input track until it aligns with the storage loops. Operating the swap gates transfers the new data into the storage loops such that consecutive bits go into adjacent loops and simultaneously transfer out the old data.

Data Output

To read data, the replicate gate is pulsed and one bit is replicated from each loop into the double period output track. The data then propagates along the output track and through the detector such that data is read out at the clock frequency.
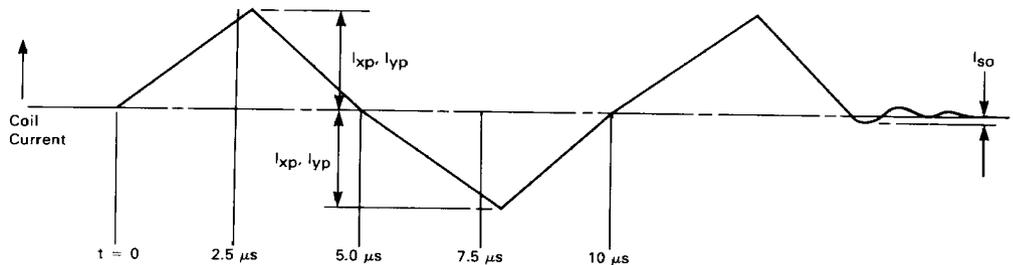
Redundancy

Of the 584 storage loops, 512 are allocated for data, 12 for error correction and 60 for redundancy. These 60 loops are used to mask inoperable minor loops and improve performance. Sixty loops are always declared redundant. Data should not be written into the redundant loops.

Redundancy Map

In addition to the 584 storage loops, the chip contains two map loops. These loops have their own transfer-in and replicate gates but share the generator and detector with the storage loops. Only one loop is required and is chosen at final test. The chosen loop is used to store the data which identifies the redundant loop map. A 'one' designates a usable loop; a 'zero,' a non-usable loop. Preceding this map code is a stream of 64 'zeros' followed by a 'one' and a 'zero' which may be used to synchronize the external control circuitry with the memory. The map loop used for storage of the redundancy information is also identified in the code (see "Coding of Redundancy Map"). Since only alternate bit positions are written into the map loop to enhance reliability, intervening bits are always zero and are ignored during read (see "Map Read Operation").

The redundancy map is also printed on the label of each device using hexadecimal format. Two digits are used per loop. Instead of providing the absolute loop number, the incremental difference between non-usable loops is printed. For example, if the first bad loop is #7, and the next two are 19 and 23, the sequence 070C04 will be printed on the label. This format allows for an incremental difference between two non-usable loops of up to 255 (FF). Loop #292 is not connected in the 1Mbit device and is always declared bad.

(b.) TYPICAL RISE/FALL IMBALANCE DUE TO DRIVE CIRCUIT

Coding of Redundancy Map. The map loop contains 1024 bits of information in five fields.

Pattern	Field	Number of Bits	Notes
MM...MM	Map Data	584	(1)
EE...EE	Error Correction	12	(2)
LL	Loop	2	(3)
UU...UU	User	360	(4)
00....0010	Sync	66	(5)

(1) Each bit corresponds to a data loop in sequence
    M = 1 identifies a usable loop (524).
    M = 0 identifies a redundant loop (60).
(2) Error correction code used is a fire code applied only to the map data.
(3) Identifies which map loop contains the redundancy information 01 — loop #1, 10 — loop #2.
(4) This field may contain factory-pertinent information. It will not contain a duplicateof the sync pattern.
(5) The sync pattern is used to locate the beginning of the map data field and identifies data page zero.

Organizational Specifications

Bits/Loop	2,048
Total Data Loops	584
Usable Data Loops	524
Error Correction Loops	12
User Data Loops	512
Total User Storage	1,048,576 bits
Map Loops	2

FUNCTIONAL DESCRIPTION

Write Data Operation

Writing data is accomplished by generating a pattern with a series of pulses applied to pins 13 and 14, starting t_{PGSF} before the swap operation. As the device continues to cycle after all data is generated, the new data and the old will be aligned at the swap gates after t_{PGSL}. A swap pulse is applied to pins 12 and 15 at this time, swapping the new data in and the old data out. The old data are propagated out and discarded beyond the active area.

Note: In order to ensure correct device operation, it is essential that at least one empty bit position follows the last bit of a data block.

Read Data Operation

To read data, the device must be cycled until the desired page is aligned with the replicate gates on the output side of the storage loops. A replicate cut pulse is applied to pins 9 and 16 to duplicate the page. This is immediately followed by a replicate transfer pulse which causes the duplicate bubbles to propagate into the output track.

Detection occurs when a bubble passes under the magnetoresistive detector element. The bubble's magnetic field causes the detector element to change resistance. By passing a constant current through the detector, this is converted to a voltage signal. A dummy detector which is not influenced by magnetic bubbles is used to cancel the background magnetoresistive signal.

Output bubbles are discarded beyond the active area after detection. A complete page is read in t_{PRDL}.

INTERFACE IMPEDANCES

Characteristics	Symbol	Min	Typ	Max	Units
Generate (2)	r_G	4.0	—	11	Ω
Swap (2)	r_S	500	—	1150	Ω
Replicate (2)	r_R	90	—	160	Ω
Map Replicate (Includes Map Transfer-In) (2)	r_M	28	—	65	Ω
Detector (Active and Reference) (2)	R_{DA}, r_{DR}	900	—	2000	Ω
Detector Active/Reference Ratio		0.985	—	1.015	
X Coil Inductance	L_X	41	—	44	μH
Y Coil Inductance	L_Y	36	—	39	μH
Z Coil Inductance	L_Z	25	—	35	μH
X Coil dc Resistance Non-Operating, 25°C	r_X	—	3.3	—	Ω
Y Coil dc Resistance Non-Operating, 25°C	r_Y	—	1.5	—	Ω
Z Coil dc Resistance Non-Operating, 25°C	r_Z	—	0.75	—	Ω
X Coil ac Resistance (2)	r_X	3.3	—	5.3	Ω
Y Coil ac Resistance (2)	r_Y	2.1	—	3.1	Ω

NOTE:
(2) $T_{C(min)}$ = 0°C, non-operating
    $T_{C(max)}$ = 70° C, operating

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OUTPUT SIGNALS (T_C = 0°C to 70°C, f_0 = 100 kHz)

Characteristic	Symbol	Min	Typ	Max	Units
Common-Mode Output Signal (I_{DA} = I_{DR} = 4.0 mA) Differential Peak-to-Peak Output Voltage (See Note 1) I_d = 4.0 mA, See Figure 1 for measurement details)	V_{cm}	—	—	50	mV
Logic 1 Bubble Present	V_{OH}	TBD	—	—	mV
Logic O No Bubble	V_{OL}	—	—	TBD	mV
Signal Strobe Leading Edge Phase	t_{so}		191		Degrees
Signal Strobe Trailing Edge Phase	t_{sc}		258		Degrees
Logic 1 Valid Window	t_{1V}	50			ns

Note 1: V_{OH} is defined as the difference between the most negative and the most positive signal excursions which occur within the phase window t_{so} to t_{sc} when a bubble is being detected. V_{OL} is similarly defined for the case of no bubble being detected. See Figure 3.

FIGURE 3
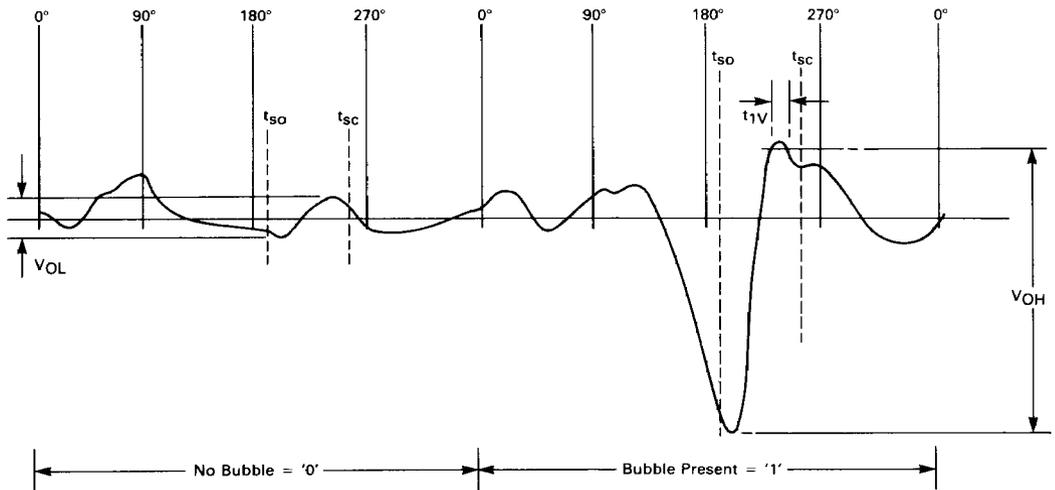
(a) DETECTOR BRIDGE OUTPUT
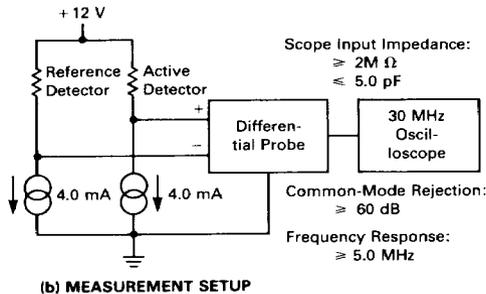
(b) MEASUREMENT SETUP

Map Read Operation

To read the contents of the map, a series of alternate cycle map replicate pulses is applied to pins 10 and 11. Data will be available after t_{PMRD}. Since map data is only loaded into alternate positions in the loop, one pass may result in no data. In this case, the procedure is repeated after delaying one cycle. The outputs from the two map loops are merged, but only one loop contains data. See "Coding of Redundancy Map Loops" for decoding information.

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Map Write Operation

Writing the map loop is accomplished by generating map information as normal data on alternate cycles. After t_{PGT1} or t_{PGT2}, pins 10 and 11 are pulsed with a series of negative map transfer pulses on alternate cycles. Selecting t_{PGT1} writes into map loop 1, selecting t_{PGT2} writes into map loop 2.

TIMING CHARACTERISTICS T_C = 0°C to 70°C, f_O = 100 kHz. See Figure 4 for test conditions. All control pulses to have rise and fall times ≤ 80 ns (10%–90% of pk amplitude) unless otherwise noted. All pulsewidths measured at 50% amplitude unless otherwise noted.

WRITE CYCLE TIMING

Characteristic	Symbol	Min	Typ	Max	Units
Generate First Bit to Swap In (1)	$t_{PGS(F)}$	—	597	—	Cycles
Generate Last Bit to Swap In (1)	$T_{PGS(L)}$	—	14	—	Cycles
Swap In to Replicate Out (1)	t_{PSR}	—	1026	—	Cycles
Swap In to Non-Volatile Storage (2)	t_{PS}	—	2	—	Cycles
Generate Delay Time (3)	t_{DG}	70		120	Degrees
Generate Pulse Width (4)	t_{WG}	100	150	200	ns
Generate Fall Time (80%–90% of pk Amplitude)	t_{FG}	200		400	ns
Swap Delay Time (3)	t_{DS}	270		330	Degrees
Swap Pulse Width	t_{WS}	340	370	400	Degrees

READ CYCLE TIMING

Characteristic	Symbol	Min	Typ	Max	Units
Replicate Out to Detect First Bit (1)	$t_{PRD(F)}$	—	91	—	Cycles
Replicate Out to Detect Last Bit (1)	$t_{PRD(L)}$	—	674	—	Cycles
Replicate Out to Swap In (1)	t_{PRS}	—	1022	—	Cycles
Replicate Delay Time (3)	t_{DR}	0		12	Degrees
Replicate Cut Pulse Width	t_{WRC}	50	75	100	ns
Replicate Transfer Pulse Width	t_{WRT}	80	100	120	Degrees

MAP READ AND WRITE CYCLE TIMING

Characteristic	Symbol	Min	Typ	Max	Units
Map Replicate to Detect	t_{PMRD}	—	97	—	Cycles
Generate to Map Loop # 1 Transfer	t_{PGT1}	—	608	—	Cycles
Generate to Map Loop #2 Transfer	t_{PGT2}	—	605	—	Cycles
Map Loop Transfer-In to Replicate	t_{PTR}	—	1028	—	Cycles
Map Replicate Delay Time (3)	t_{DRM}	0	—	12	Degrees
Map Replicate Cut Pulse Width	t_{WRCM}	50	75	100	ns
Map Replicate Transfer Pulse Width	t_{WRTM}	80	100	120	Degrees
Map Transfer-In Delay Time	t_{DTM}	270	—	330	Degrees
Map Transfer-In Pulse Width	t_{WTM}	200	220	240	Degrees

NOTES: (1) Propagation times are defined from the beginning of the cycle in which the first signal occurs to the beginning of the cycle in which the second signal occurs.
(2) Data is non-volatile at the end of the cycle in which the swap current is turned off.
(3) These parameter limits are guaranteed when the device is driven with the X and Y current shown in Figure 4. Deviations from these drive conditions may cause these limits to change in absolute angle, but the phase range (max.–min.) will remain as specified.
(4) Generate pulse width is defined from 50% amplitude on the rising edge to 90% amplitude on the falling edge.

Bubble

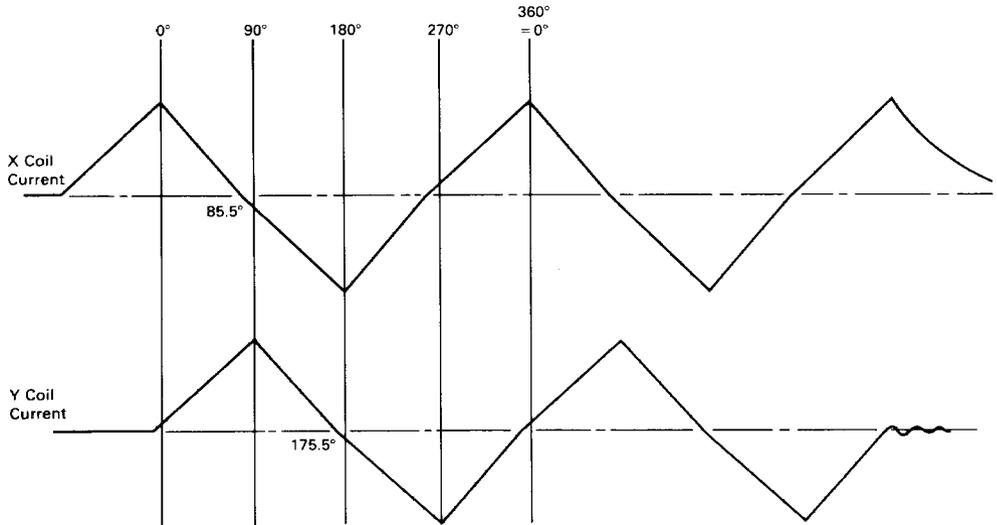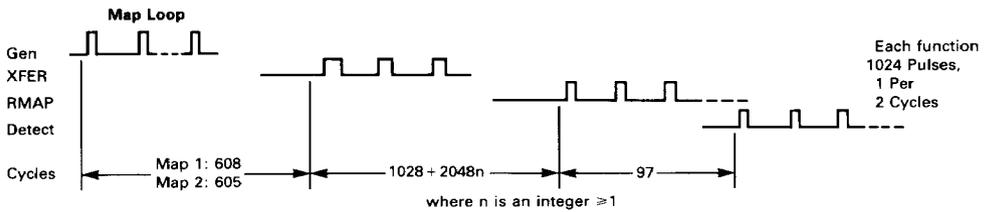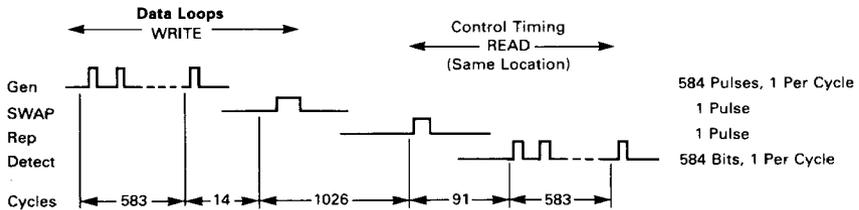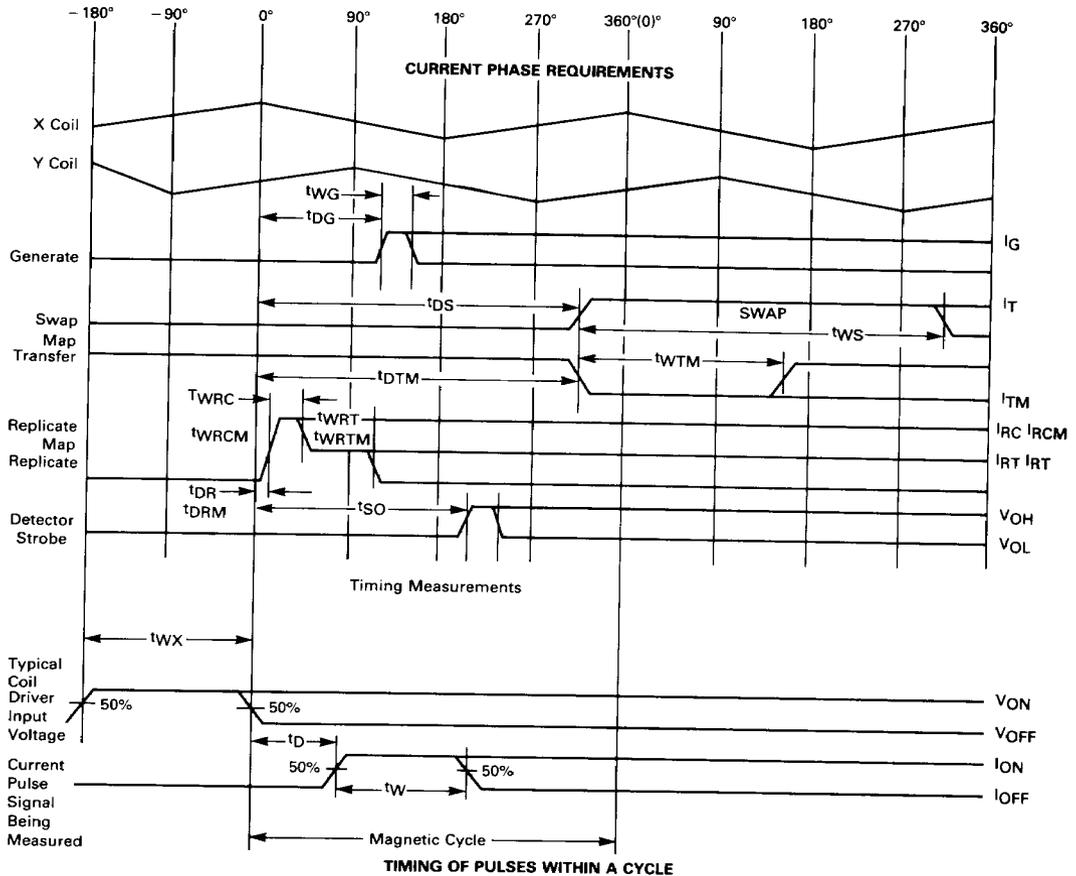**FIGURE 4 — TEST CONDITIONS — X AND Y CURRENT WAVEFORMS**

FIGURE 5

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FIGURE 6 — X, Y COIL TIMING

MECHANICAL SPECIFICATION

Package

The MBM2011A device is a 16-pin dual-in-line package. The die is mounted on a printed circuit board carrier attached to a beryllium copper leadframe and encapsulated in plastic compound. Two orthogonal coils and a pair of permanent magnets enclose the die and the whole device is molded into a Mumetal shield. A Z coil is included in the device to facilitate testing and extended temperature range operation.

Mechanical Data

Package Size	1.15 x 1.10 x 0.36 in (29.2 x 27.9 x 9.14) mm
Package Weight	28 gm.

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ENVIRONMENTAL SPECIFICATION

Temperature Ranges

(See "Absolute Maximum Ratings").

External Magnetic Fields

When subjected to an external magnetic field of 20 Oe maximum in any direction the device will continue to operate satisfactorily as long as the parameters are kept within the range specified in this document.

Screen Tests	All Parts 100%
Die Visual	100X Inspection consistent with MIL-883B, Method 2010, Cond. B
Stabilization Bake	As per MIL-STD-883B, Method 1008, Condition C, 150°C for 24 hours
Temperature Cycling	As per MIL-STD-883B, Method 1010, Condition B, 10 cycles −55°C → 125°C
External Visual	MIL-883B, Method 2009

Qualification Testing

Bond Strength	MIL-883B, Method 2011.3, Condition D
Mechanical Shock	MIL-883B, Method 2002, Condition B: 1,500G for 0.5 ms
Variable Frequency	MIL-883, Method 2007, Condition A: 20-2,000 Hz for 4 mins.; peak at 20 G's.
Thermal Shock	MIL-883, Method 1011.3, Condition B: −55°C to 125°C, 15 cycles
Moisture Resistance	MIL-883B, Method D 1004.3
Resistance to Solvent	MIL-883B, Method 2015.1
Solderability	MIL-883B, Method 2003.2
Lead Integrity	MIL-883B, Method 2004.3
Flammability	Needle Flame, IEC 695-2-2

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